REMARKS

Claims 1 to 21 and 23 to 29 are pending in this application. Claims 1, 9, 18, 21 and 25 are the independent claims. Claim 29 is new. Favorable reconsideration and further examination are respectfully requested.

Initially, Applicants thank the Examiner for conducting an interview on Wednesday, February 27, 2008. The Examiner indicated that FIFO buffer 408 is an alignment buffer and that 3DES CBC unit 410 is a crypto system. Applicants explained to the Examiner that FIFO buffer 408 is not an alignment buffer because no alignment was being done by the FIFO buffer 408 rather alignment was being done by a data align barrel shifter 404. No agreement was reached between the Examiner and the Applicants on the claims.

Claims 1, 2, 5 to 8, 21, 23 to 25, 27 and 28 were rejected under 35 U.S.C. §103(a) as being obvious by Elnathan et al. (U.S. Patent Number 7,245,616 hereinafter "Elnathan") in view of Krishna et al. (U.S. Patent Number 6,477,646 hereinafter "Krishna") and in view of Vandenhoudt et al. (U.S. Patent Publication Number 2003/0002509 hereinafter "Vandenhoudt").

Claim 1 is directed to a processor. The processor includes a crypto system, an alignment buffer to receive header data and ciphered data from the crypto system, the crypto system encrypting data to form ciphered data so that an intended receiver with a correct cryptographic key may decrypt the ciphered data and a switch fabric having a plurality of transmit buffer elements to receive data from the alignment buffer. The alignment buffer provides data to the switch fabric in blocks having a predetermined size.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1. In particular, the cite art does not disclose or suggest an alignment buffer to receive header data and ciphered data from the crypto system and provides data to the switch fabric in blocks having a predetermined size.

As acknowledged by the Examiner, neither Elnathan nor Vandenhoudt teach an alignment buffer to receive header data and ciphered data from the crypto system and provide data to the switch fabric in blocks having a predetermined size.

To make-up for the deficiencies in Elnathan and Vandenhoudt of not teaching an alignment buffer to receive header data and ciphered data from the crypto system and provide data to the switch fabric in blocks having a predetermined size, the Examiner has cited Krishna. As indicated in the aforementioned teleconference the Examiner has indicated that FIFO buffer 408 is an alignment buffer. Applicants respectfully disagree. The FIFO buffer 408 is not an alignment buffer because no alignment is being done by the FIFO buffer 408, but rather alignment is being done in Krishna by a data align barrel shifter 404. Moreover, Applicants have clearly defined in the specification what an alignment buffer does. Therefore, Krishna does not disclose or suggest an alignment buffer to receive header data and ciphered data from the crypto system and provide data to the switch fabric in blocks having a predetermined size.

Accordingly, for at least the reasons indicated above, even if Krishna were combined with Elnathan and Vandenhoudt, the resulting hypothetical combination would not disclose or suggest an alignment buffer to receive header data and ciphered data from the crypto system and provide data to the switch fabric in blocks having a predetermined size. For at least this reason, claim 1 is believed to be allowable.

Claims 9, 18, 21 and 25 include the corresponding feature in claim 1 of an alignment buffer to receive header data and ciphered data from the crypto system and provide data to the switch fabric in blocks having a predetermined size 1. Applicants submit that the Elnathan, Vandenhoudt and the Krishna references should also be withdrawn with respect to claims 9, 18, 21 and 25 for at least the same reasons as claim 1.

Applicants also submit that independent claim 21 and dependent claims 6 and 26 are further distinguished from the cited prior art. In particular, the cited art does not disclose or suggest that the crypto system includes a plurality of crypto unit processing contexts and the alignment buffer includes a number of buffer elements equal to a number of processing contexts. Applicants respectfully submit that that Krishna does not disclose or suggest that the FIFO 408 buffer includes buffer elements much less that the number of buffer elements is equal to a number of processing contexts. Furthermore, the cited art does not disclose other features of claim 6, 21 and 26 such as the plurality of processing contexts are configured to process at least one data packet at a time and to store cipher keys and algorithm context associated with processing the at least one data packet.

With respect to claim 7, Applicants submit that the cited art does not disclose or suggest that the crypto system includes a plurality of cipher cores. Krishna merely shows a single crypto unit, 3DES CBC unit 410 connected to the FIFO buffer 408. Therefore, Applicants submit that claim 7 is allowable.

Moreover, the cited art does not disclose or suggests that an alignment buffer has a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units as recited in claim 18.

As acknowledged by the Examiner, neither Elnathan nor Vandenhoudt does not teach an alignment buffer having a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units.

To make-up for the deficiencies in Elnathan and Vandenhoudt of not teaching an alignment buffer having a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units, the Examiner has cited Krishna. As indicated in the aforementioned teleconference the Examiner has indicated that FIFO buffer 408 is an alignment buffer and that 3DES CBC unit 410 is a crypto system. Krishna only shows a single crypto unit not a first and second crypto units. Moreover, Krishna does not teach a plurality of processing contexts much less a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units. Therefore Krishna does not disclose or suggest that an alignment buffer having a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units.

Accordingly, for at least the reasons indicated above, even if Krishna were combined with Elnathan and Vandenhoudt, the resulting hypothetical combination would not disclose or suggest an alignment buffer having a respective element for each of the plurality of processing contexts to receive the ciphered data from the first and second crypto units. For at least this reason, claim 18 is believed to be allowable.

With respect to new claim 29, Applicants further submit that the cited art does not disclose or suggest that the plurality of processing contexts are configured to allow latency of loading cryptographic key material and packet data to be hidden by pipelining loading of the

packet data and the key material into a first portion of the plurality of processing contexts with processing of the packet data in a second portion of the plurality of processing contexts. Therefore, Applicants submit that claim 29 is also allowable.

For at least the foregoing reasons, Applicants request withdrawal of the art rejection.

Applicants submit that all dependent claims now depend on allowable independent claims.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for withdrawing the prior art cited with regards to any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Applicants submit that the entire application is now in condition for allowance. Such action is respectfully requested at the Examiner's earliest convenience.

Applicants' attorney can be reached by telephone at (781) 401-9988 ext. 123.

No fee is believed to be due for this Response; however, if any fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: INTEL-014PUS.

Respectfully submitted,

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